Requirements of the CKM QIE and the Associated R&D for 2002.

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Abstract

The requirments of the pipelined charge integrating encoder for the CKM experiment are described, along with the expected R&D to demonstrate the required performance.

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1 Introduction.

The recently approved CKM experiment is a high-rate counter based experiment that requires a high speed readout of fast (10 nsec FWHM, 2 nsec risetime) PMT pulses. The success of the experiment hinges on maintaining very low detection inefficiency ($< 1 \times 10^{-5}$) of these PMT pulses. To achieve this low level of detection inefficiency we have developed a conceptual design that has redundant parallel readout of the PMT pulse with a TDC and a charged integrating encoder. Details of this design and the detector systems can be found in the CKM scientific proposal (April 2001). In this design the last dynode of the PMT is instrumented with an on-base discriminator circuit that drives an LVDS signal into a nearby (10m) TDC channel. The anode of the PMT drives the negative charge pulse into a 10m long 50-ohm RG-58 cable that terminates at the input of the charge integrating circuitry. It appears plausible that the CMS QIE ASIC with modest variations could be employed to meet the experiments requirements. These requirements and described below.

2 Required Dynamic Range:

There are two main detector systems that will have their PMTs anode charged digitized. The first system, the "Vacuum Veto System" (VVS) presents a charge dynamic range from 40 fC, (0.25 MeV deposited LSB) to 320 pC, (2 GeV deposited). This corresponds to a dynamic range of $\times 8000$. The other system is the "Forward Veto System" (FVS) which presents a charge dynamic range from 10 fC, (2 MeV deposited LSB) to 75 pC, (15 GeV deposited) which corresponds to a dynamic range of $\times 7500$. The dynamic range of the non-inverting input of the CMS QIE is 2.7 fC (LSB)$\times 10,000$ $=$ 27 pC. Although the required span of the VVS and FVS are both less than $\times 10,000$, the inputs will have to be correspondingly attenuated in order to observe the current maximum charge performance of the CMS QIE IC.

3 Required Sensitivity:

The CMS QIE operating with the non-inverting input has achieved a RMS noise figure of $\sim 2fC$ (with 3m cable) on the bench (personal communication, Tom Z.). This is clearly far below the required LSB of both systems. In order to match the input sensitivity of the current CMS QIE, the input VVS channels will have to be attenuated by $\sim \times 15$, and the input FVS channels will have to attenuated by $\sim \times 3$. This margin of input attenuation may be useful in realizing the required speed performance as discussed later.

4 Required Speed:

In order to extract timing information from the fast PMT pulses (FWHM 10 nsec), the digitizer needs to operate at an effective speed of 80-100 MHz. The CMS part is designed to operated at 40 MHz, and hence a significant redesign of the CMS design will be required to achieve this performance in a single IC design. One can consider an alternate design based on two devices operating in parallel on opposite clock phases that can effectively reach a sampling frequency of 2×40MHz. The viability of this design concept is now being studied. It is clear that DC-coupling of two QIE inputs to the same anode is problematic, and the excess gain of the input PMT source could be exploited to partially isolate the QIE from one another through the required input attenuation network.

5 Required Precision:

The VVS has an intrinsic detector resolution of ($> 8\%$) and the FVS has an intrinsic resolution of ($> 2\%$). In order for the (5^{+})-bit precision of the QIE readout not to contribute significantly to the measured resolution function, the QIE mantissa will have to be increased from 5 to 6 bits.

6 Phase Sensitivity:

The CKM experiment operates in a high intensity charged kaon beam that has no significant clock structure. This is required in order to minimize pile-up rate effects. Operating a QIE device in this environment is a significant departure from all previous applications where the beam was clocked, and where the QIE could be clocked at the same frequency. In the CKM application the fast charge pulse arrives at a random phase with respect top the digitization clock, and hence the integrated charge of 3 contiguous slices must be independent of clock phase. The CKM specification for phase sensitvity on the sum of 3 contiguous slices is less than $\pm 1\%$ uncorrected, and up to $\pm 2\%$ if a straightforward linear phase correction can be applied.

7 Input Impedence Profile:

The simplest implemenation of a CMS-QIE based readout system would be conventional multi-channel PCB boards where the inputs are 10m from the the PMT anodes. Given this cable run it is important for the QIE input impedence to match the impedence of the input 50-ohm cable to $\pm 2\%$ so that reflections are minimized. This performance has been achieved on the bench for most of the input dynamic range. (Personal communication, Tom Z.)

8 Required work for calander 2002:

An important near-term goal for CKM is the submission of a Technical Design Report by early 2003. To reach this end, there are two main QIE realted efforts that must be pushed. These efforts are the design of a CMS-QIE based prototype system that can achieve an effective operation frequency of 80-100 MHz, and the instrumenation of an 8-channel VVS prototype that will be exposed to an electron test beam in October of 2002. The speed prototype studies can and should be carried out on the bench independent of the test beam effort. The test beam effort will use existing Version-1 CMS-QIE parts operating on a variant of the CMS-QIE test board that is under development now for CMS. The test beam effort will operate eight QIE input channels instrumenting 8 PMT anodes with an appropriate attenuation network to achieve the required charge sensitivity. The eight channels will operate at the maximum frequency allowed by the existing parts.